REMARKS

Present Status of the Application

The Office Action mailed April 05, 2002 rejected all presently-pending claims 1, 3-8, and 10-11. Specifically, claims 1-4, 7, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshikawa, U.S. Patent No. 6,335,554. Claim 5-6, 11-12 are rejected under 35 U.S.C.103(a) as being unpatentable over Yoshikawa, U.S. Patent No. 6,340,827. Claims 8-9 are rejected under 35 U.S.C.112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

After entry of the foregoing amendments, claims 1, 3-8, and 10-11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The present invention provides a structure of a flash memory, which reduces the amount of variation of the threshold voltage and enhances data retention of the flash memory. The present invention also provides a structure of a flash memory comprising an electron trapping layer, a gate and a source/drain region, wherein the electron trapping layer is formed by stacking in sequence a first oxide layer and a dielectric layer with a high dielectric constant (i.e. a dielectric

constant higher than that of Si_3N_4/SiO_2, also known as NO). The gate is arranged on the electron trapping layer, and the source/drain region is arranged on the substrate of the two lateral sides of the electron trapping layer. In addition, the band gap of the material used for the high dielectric constant dielectric layer determines whether or not a second oxide layer should be provided on the high dielectric constant dielectric layer. The second oxide layer is not needed if the band gap of the high dielectric constant dielectric layer is closer to or greater than that of silicon oxide. On the other hand, a second oxide layer is needed if the band gap is smaller than that of silicon oxide. The advantage of the present invention is that a high dielectric constant material is used as the main material for the dielectric layer. Thus, the amount of variation of the threshold voltage is greatly reduced, and data retention of the flash memory is enhanced.

Discussion of Office Action Rejections under 35 U.S.C. 102(e) over Yoshikawa

A preliminary discussion of the differences between the technology and structure disclosed in Yoshikawa and the present invention is appropriate. In this regard, there is a fundamental difference in the structure and technique. Yoshikawa is directed to a conventional nonvolatile memory such as EEPROM with two charge trapping layers formed on both sides of the gate electrode where they are perfectly electrically separated from each other through the second gate

insulation film, as indicated in FIG. 4. In contrast, the present invention forms a uniform electron trapping layer entirely over the surface of semiconductor. The electron trapping layer comprises of a stacked layer of a first oxide layer, a special high-dielectric constant layer, and an additional second oxide layer. Yoshikawa teaches away from the present invention by having the charge trapping layers forming extensionally from the end of the gate electrode to a channel area direction. Yoshikawa teaches that the current transmission characteristics of the memory cell is substantially determined in accordance with the charge trapping state in the portion on the channel area side of the charge trapping layers. It is clear that Yoshikawa does not anticipate the present invention because Yoshikawa teaches to have the charge trapping layers growing on both ends of the gate instead of uniformly underneath the gate as taught in the present invention. Furthermore Yoshikawa discloses the mandatory use of a third dielectric layer with also a high dielectric constant that separates the charge trapping layers and the gate so the structure is more complicated and increases manufacturing cost. The present invention can selectively deposit the second oxide layer according to the band gap of the material of the high dielectric-constant layer. Therefore Yoshikawa is clearly teaching away from the present invention by having the trapping layers formed on both ends of the gate and electrically isolated from each other. Yoshikawa does not disclose any information regarding the second oxide layer having a band

gap that is smaller than that of SiO_2 as cited in claim 1. As from the above arguments and evidence of the technical difference and teaching away from Yoshikawa, Yoshikawa is not a proper cited reference to reject claims 1-4, 7 and 10.

Discussion of Office Action Rejections under 35 U.S.C. 102(e) over Shimoji

A preliminary discussion of the differences between the technology and structure disclosed in Shimoji and the present invention is appropriate. In this regard, there is a fundamental difference in the structure and technique. Shimoji is directed to a nonvolatile semiconductor device having charge trap film containing silicon crystal grains. The silicon crystals in a thermal oxide film can alter the dielectric constant of the charge trap film because the silicon grains can suppress the generation of depletion layers. The charge trapping layers containing silicon crystals can improve the signal charge holding property of the charge trap film in comparison with a silicon nitride film. As a result, Shimoji also explicitly teaches away from the present invention having a layer with a material that has an inherent high dielectric constant by using silicon crystals in the charge trapping layer. Shimoji teaches to use silicon crystal because of its inherent characteristics which can improve the signal charge holding property of the charge trap film by suppressing generation of depletion layers. Shimoji does not disclose

the use of any material such as Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2 that has a natural high dielectric constant as cited in claim 7. Shimoji and the present invention both solve the same problem of improving charge trapping but by different methods and therefore because they take mutually exclusive paths in reaching different solutions to similar problem, they teach away from each other and it would be illogical to combine them. Therefore Shimoji is not a proper cited reference to reject claim 7.

Discussion of Office Action Rejections under 35 U.S.C. 103(a) over Yoshikawa and Choi

As indicated in the aforementioned discussion of office action rejection under U.S.C 102(e) over Yoshikawa, Yoshikawa teaches away from the present invention and therefore "a person of ordinary skill, upon reading the reference, would be led in a direction divergent from the path that was taken by the applicant.", see ***In re Gurley***, 27 F.3d 551, USPQ 2d 1130, 1131 (Fed. Cir. 1994). As a result, there is no motivation or suggestion to combine Yoshikawa with Choi. Choi teaches diffusion barrier for use with high dielectric constant for preventing the migration of oxygen into the high dielectric constant layer during heat treatment. Choi teaches an improved diffusion barrier for a high dielectric constant but does not disclose any information on using a high dielectric constant layer in a memory structure for reducing the amount of variation

of the threshold voltage and enhancing the data retention of the flash memory. As a result, there is no suggestion or motivation in either Yoshikawa or Choi to combine as stated in the office action being "a mere substitution of art-recognized equivalent values".

Furthermore there is no proper teaching or suggestion to combine Yoshikawa and Choi. The Applicants would like to indicate that the establishment of the prima facie case of obviousness is improper because the Examiner failed to provide the reason supporting the suggestion or motivation to combine. It is argued that the Examiner used the present invention and hindsight as the source of suggestion to combine the prior art. In this regard, it is well settled law that in order to properly support an obviousness rejection under 35 U.S.C 103, there must have been some teaching in the prior art to suggest one skilled in the art that the claimed invention would have been obvious. See ***W.L. Gore & Associates, Inc. v. Garlock Thomas, Inc.*** 721 F.2d 1540, 1551 (Fed. Cir. 1983). Also see ***In re Dow Chemical Company***, 837 F.2d 469, 473 (Fed. Cir. 1988) In this regard, the Applicants note that there must not only be a suggestion to combine functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. In regard to response to arguments in the Office Action, the Applicants would like to refer to ***Stiftung v. Renishaw*** PLC, 945 Fed.2d 1173 (Fed.

Cir. 1991). In order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements and not base upon hindsight reasoning unsupported by the prior art themselves.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1, 3-8, and 10-11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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Date: 9/25/2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Claims:

Claims 2, 9, and 12 have been canceled without prejudice and disclaimer.

Claims 1 and 7 have been amended as follows:

1. (Once Amended) A structure of a flash memory comprising:

a first oxide layer positioned on a substrate;

a dielectric layer having a high dielectric constant positioned on the first oxide layer;

a second oxide layer positioned on the dielectric layer having the high dielectric constant, wherein the first oxide layer, the dielectric layer having the high dielectric constant and the second oxide layer together form a charge trapping layer, wherein a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide (SiO_2); and

gate located on the second oxide layer of the charge trapping layer; and

a source/drain region located at two lateral sides of the substrate.

7. (Once Amended) A structure of a flash memory comprising:

a first oxide layer positioned on a substrate;

a dielectric layer having a high dielectric constant positioned on the first oxide layer, wherein the dielectric layer and the first oxide layer together form a charge trapping layer and the dielectric layer having the high dielectric constant is a mixture of materials selected from a group consisting of Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2; [and]

a gate positioned on the dielectric layer having the high dielectric constant; and

a source/drain region positioned at two lateral sides of the substrate.